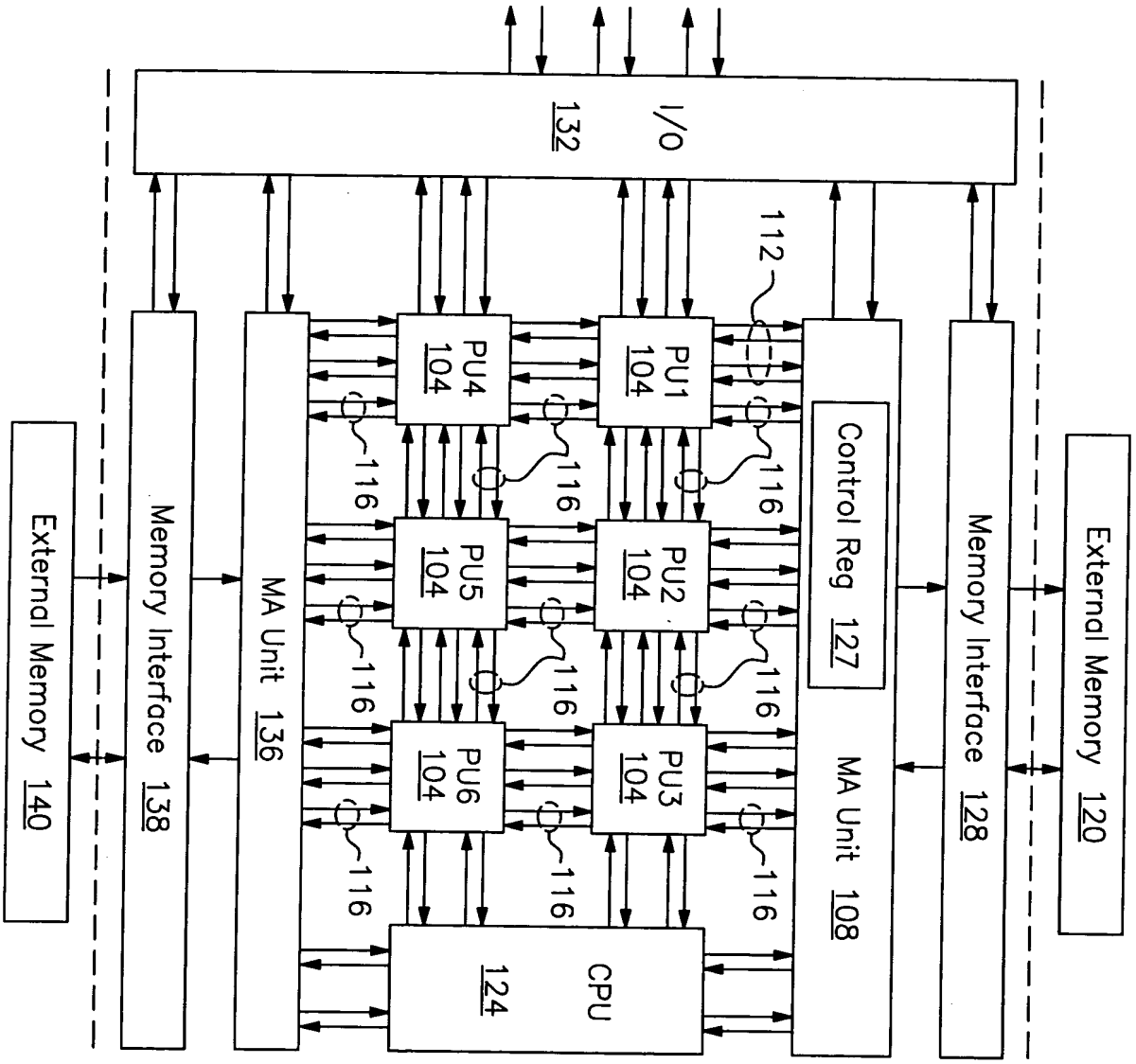

Fig. 1

Blakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800
Title: CONTROLLING MEMORY ACCESS DEVICES IN A DATA DRIVEN ARCHITECTURE MESH ARRAY
1st Named Inventor: Louis A. Lippincott
Express Mail No.: EV339917539US Docket No.: 42P17013
Sheet: 1 of 11

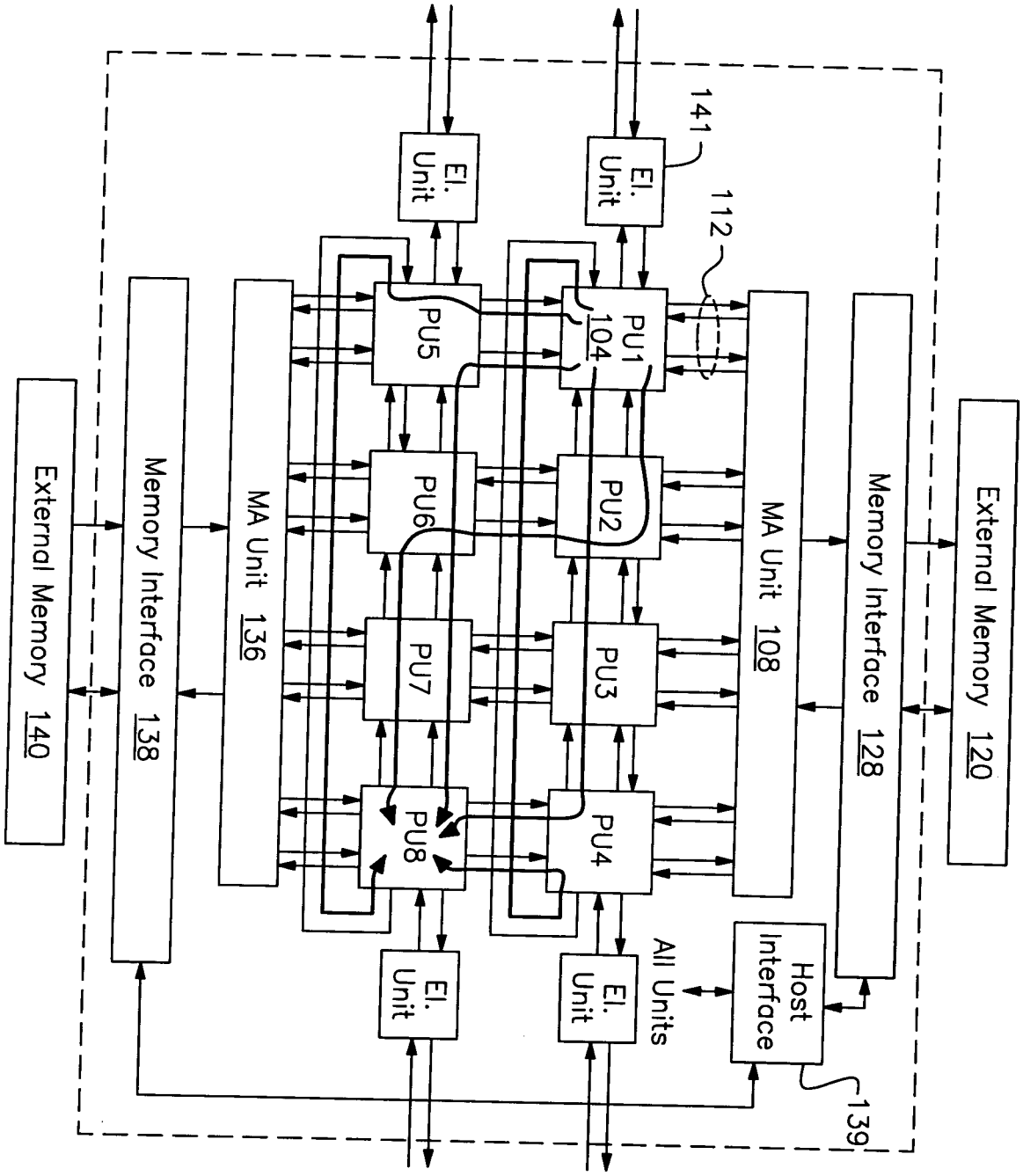
External Memory 120
Memory Interface 128
MA Unit 108
Memory Interface 138
MA Unit 136
External Memory 140
El. Unit
141
112
PU1 104
PU2
PU3
PU4
PU5
PU6
PU7
PU8
All Units
Host Interface
139

Fig. 2

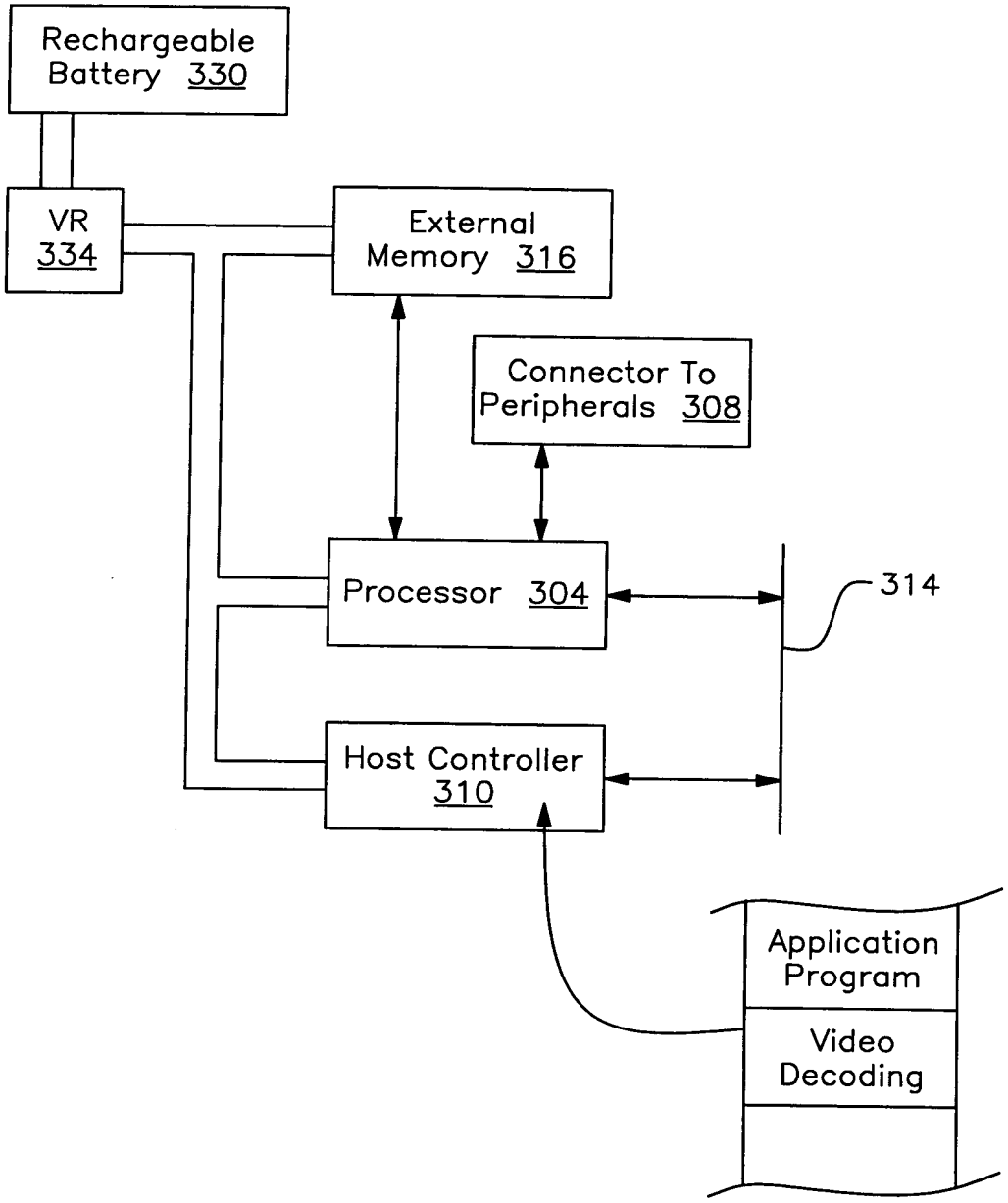
Rechargeable Battery 330
VR 334
External Memory 316
Connector To Peripherals 308
Processor 304
314
Host Controller 310
Application Program
Video Decoding

Fig. 3

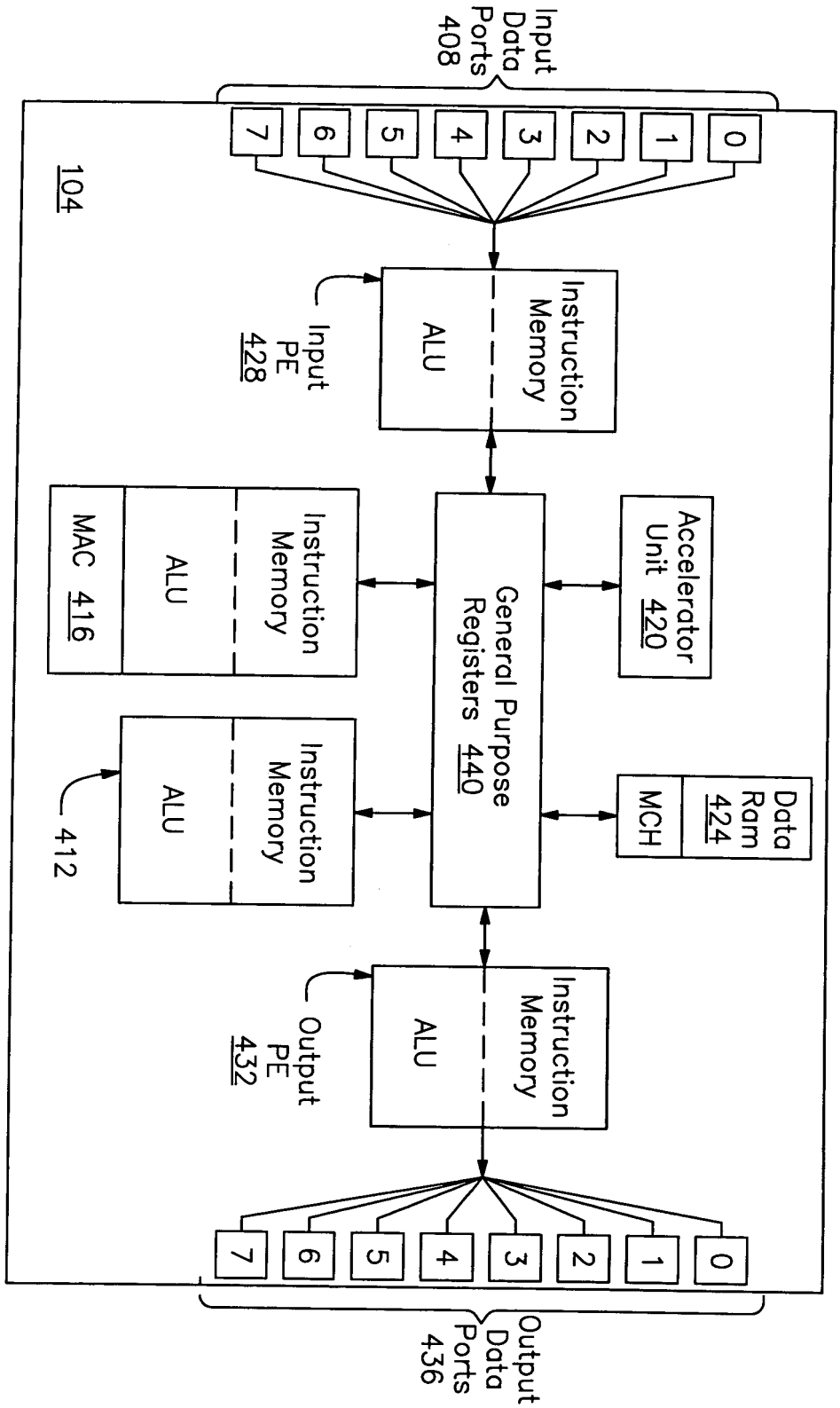
Input Data Ports 408
7
6
5
4
3
2
1
0
104
Input PE 428
ALU
Instruction Memory
Accelerator Unit 420
General Purpose Registers 440
MAC 416
ALU
Instruction Memory
412
ALU
Instruction Memory
MCH
Data Ram 424
Output PE 432
ALU
Instruction Memory
7
6
5
4
3
2
1
0
Output Data Ports 436

Fig. 4

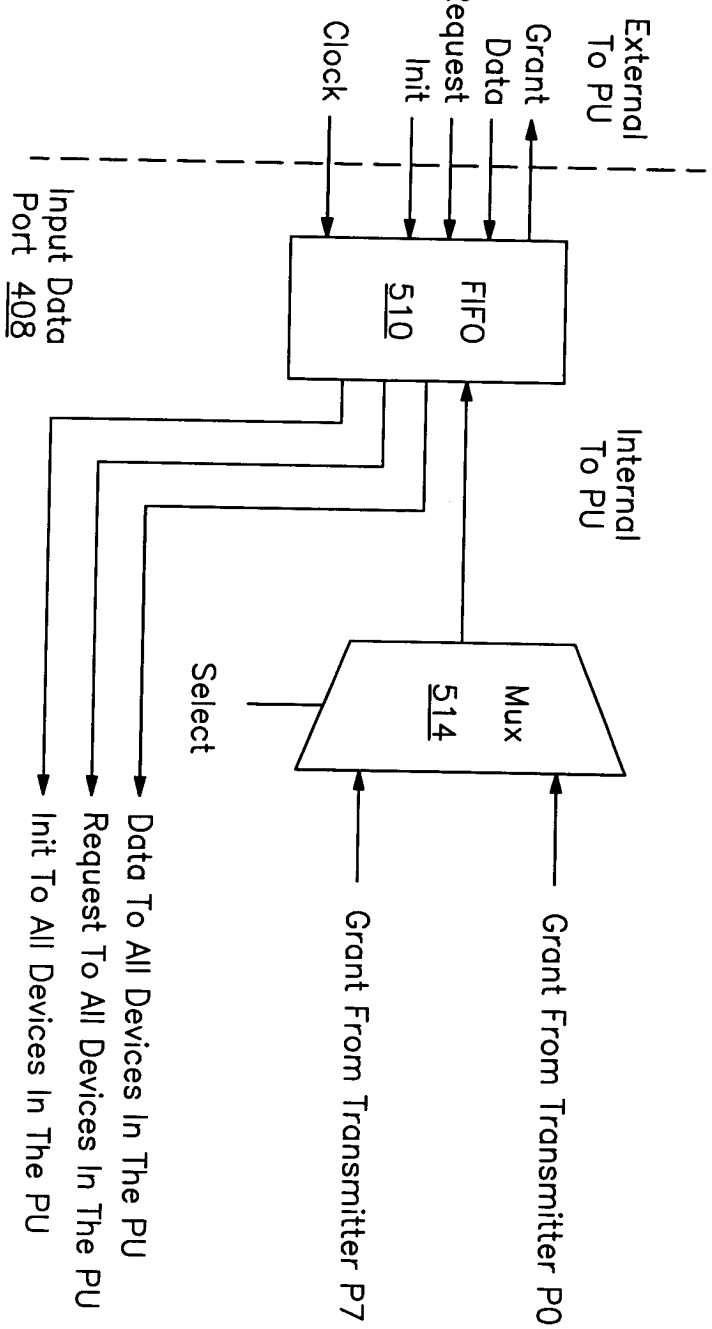
External To PU
Grant
Data
Request
Init
Clock
Input Data Port 408
FIFO 510
Internal To PU
Mux 514
Select
Grant From Transmitter P0
Grant From Transmitter P7
Data To All Devices In The PU
Request To All Devices In The PU
Init To All Devices In The PU

Fig. 5

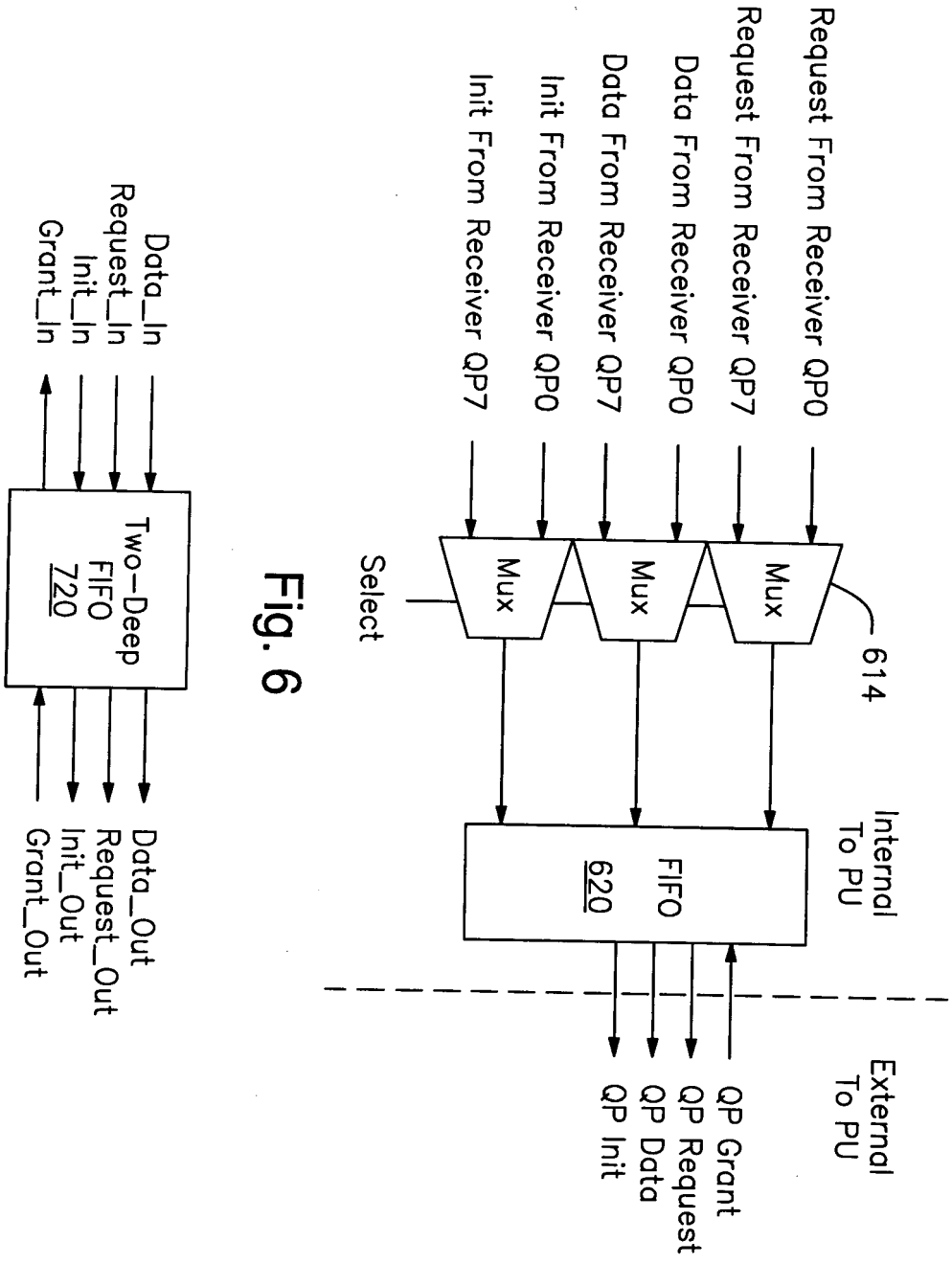
Request From Receiver QP0
Request From Receiver QP7
Data From Receiver QP0
Data From Receiver QP7
Init From Receiver QP0
Init From Receiver QP7
Select
Mux
Mux
Mux
614
FIFO
620
Internal To PU
External To PU
QP Grant
QP Request
QP Data
QP Init

Fig. 6

Data_In
Request_In
Init_In
Grant_In
Two-Deep FIFO 720
Data_Out
Request_Out
Init_Out
Grant_Out

Fig. 7

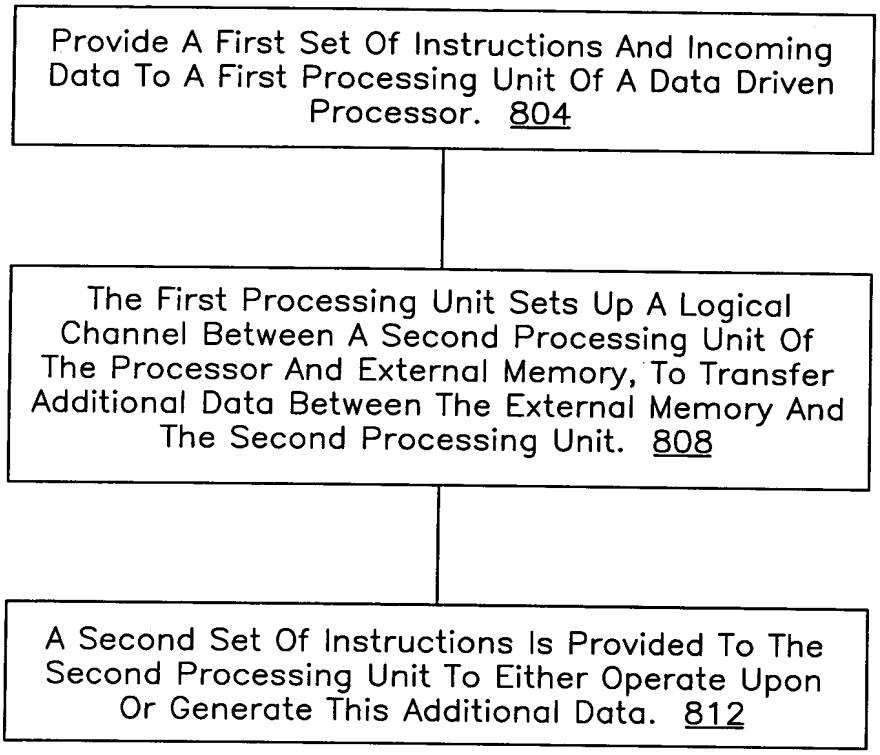
Provide A First Set Of Instructions And Incoming Data To A First Processing Unit Of A Data Driven Processor. 804
The First Processing Unit Sets Up A Logical Channel Between A Second Processing Unit Of The Processor And External Memory, To Transfer Additional Data Between The External Memory And The Second Processing Unit. 808
A Second Set Of Instructions Is Provided To The Second Processing Unit To Either Operate Upon Or Generate This Additional Data. 812

Fig. 8

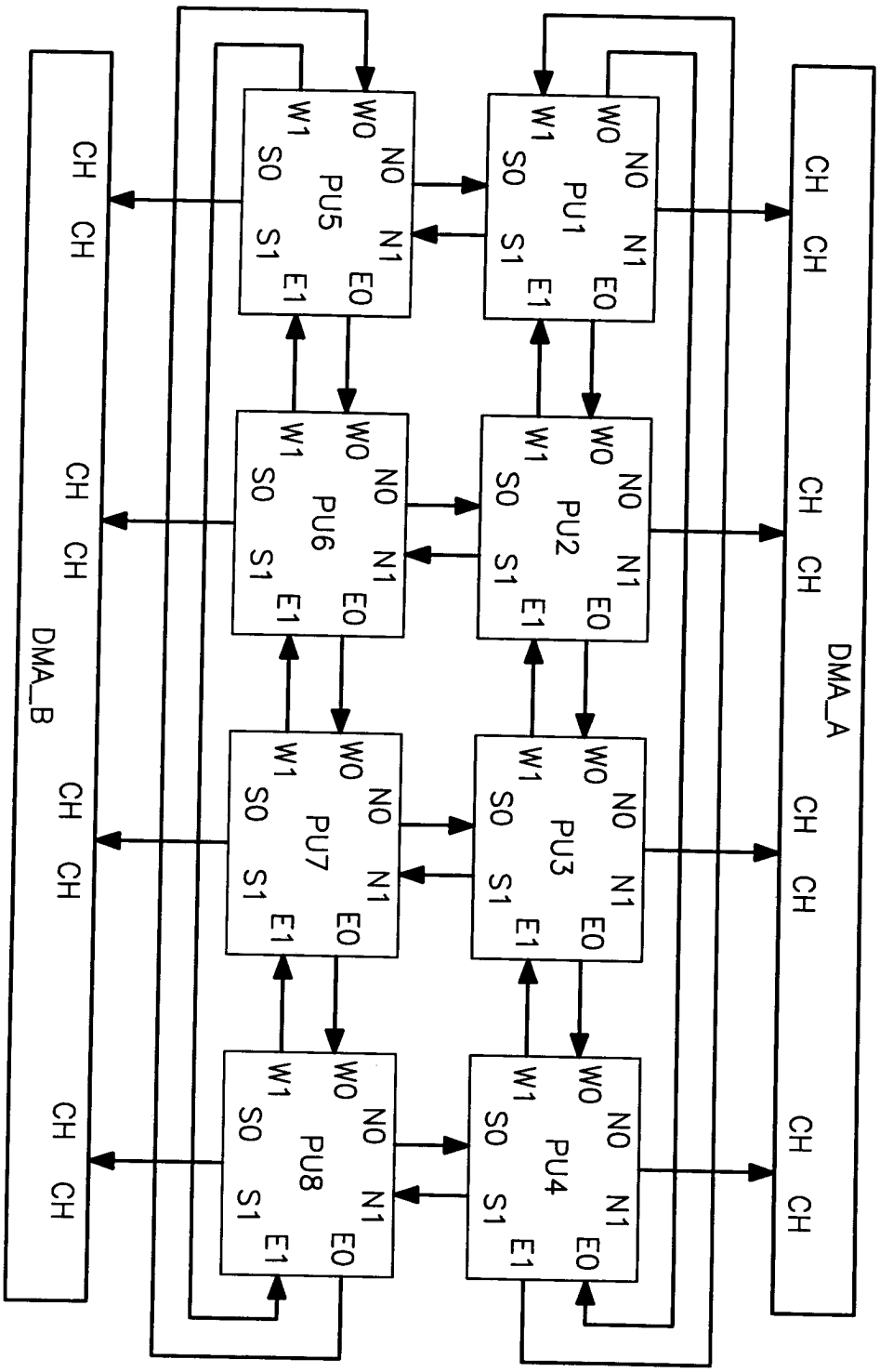
DMA_B
DMA_A
CH
PU5
PU1
PU6
PU2
PU7
PU3
PU8
PU4
W0
W1
N0
N1
S0
S1
E0
E1

Fig. 9

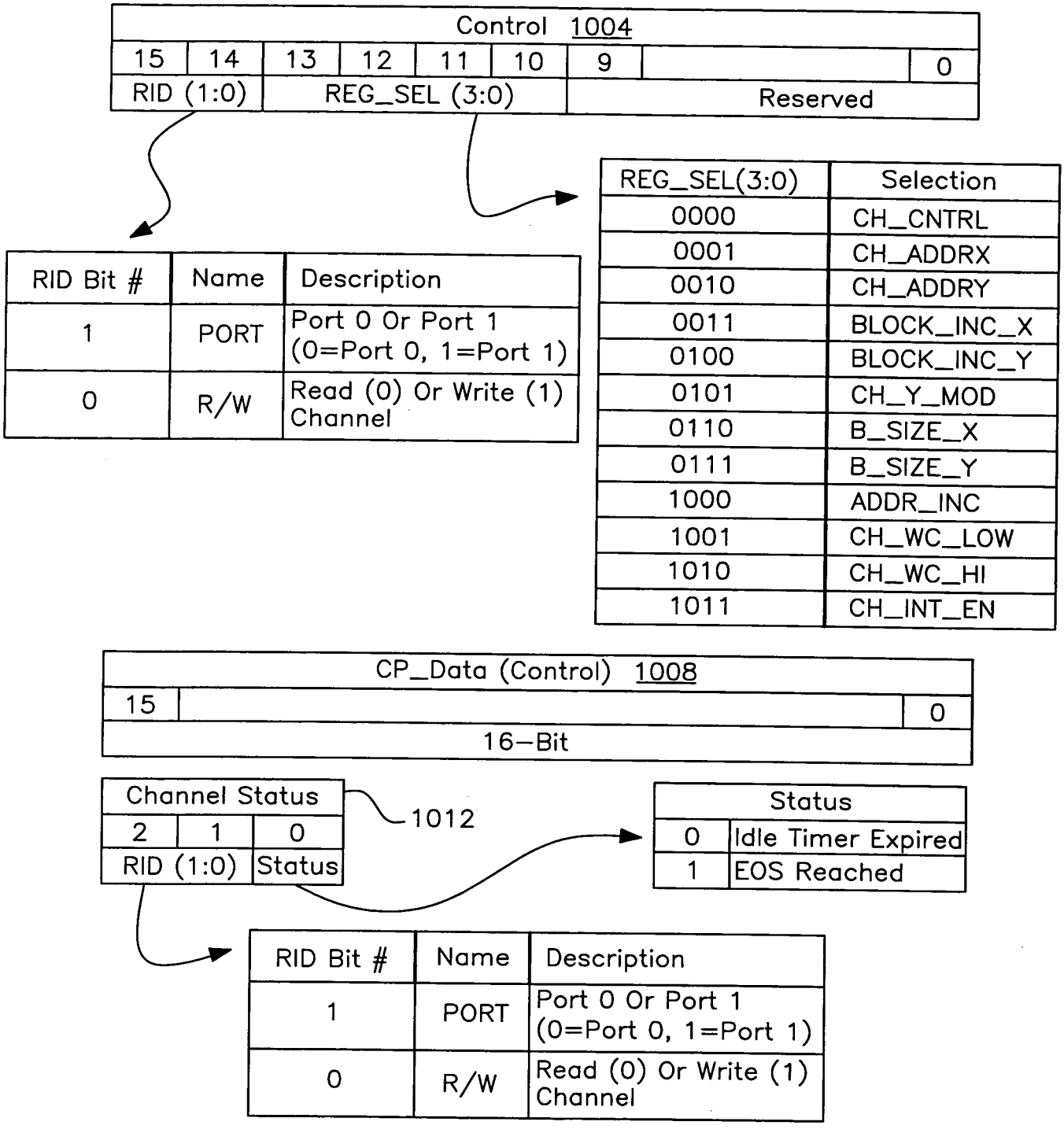
Control 1004
15 14 13 12 11 10 9 0
RID (1:0)
REG_SEL (3:0)
Reserved
RID Bit # | Name | Description
1 | PORT | Port 0 Or Port 1 (0=Port 0, 1=Port 1)
0 | R/W | Read (0) Or Write (1) Channel
REG_SEL(3:0) | Selection
0000 | CH_CNTRL
0001 | CH_ADDRX
0010 | CH_ADDRY
0011 | BLOCK_INC_X
0100 | BLOCK_INC_Y
0101 | CH_Y_MOD
0110 | B_SIZE_X
0111 | B_SIZE_Y
1000 | ADDR_INC
1001 | CH_WC_LOW
1010 | CH_WC_HI
1011 | CH_INT_EN
CP_Data (Control) 1008
15 0
16-Bit
Channel Status
2 1 0
RID (1:0) Status
1012
Status
0 Idle Timer Expired
1 EOS Reached
RID Bit # | Name | Description
1 | PORT | Port 0 Or Port 1 (0=Port 0, 1=Port 1)
0 | R/W | Read (0) Or Write (1) Channel

Fig. 10

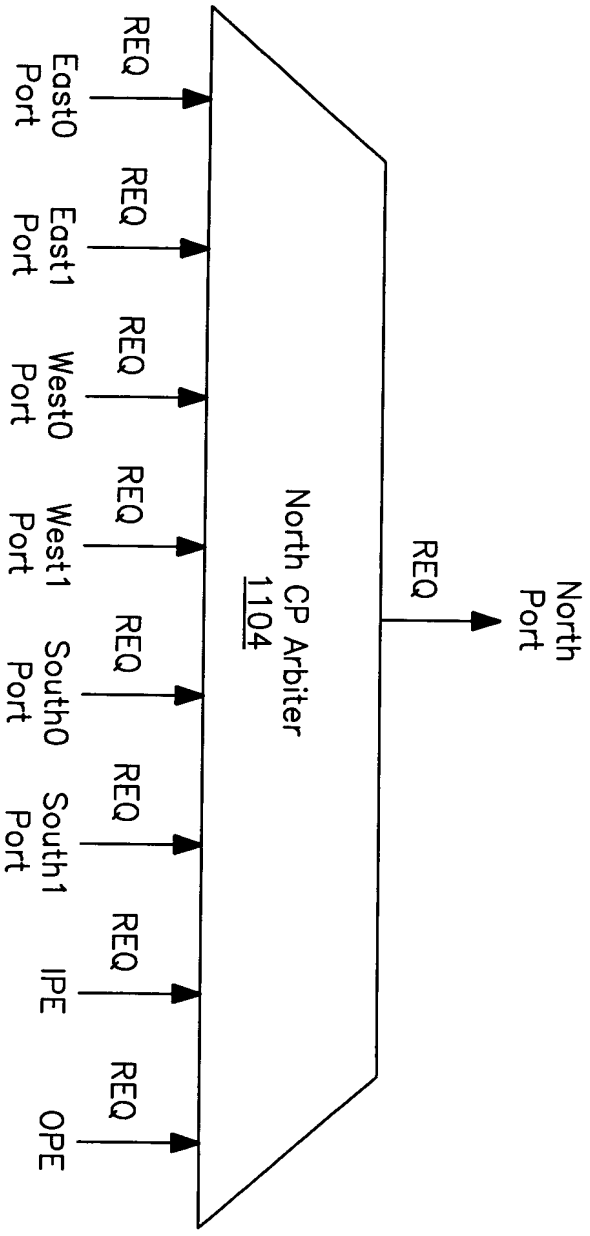
REQ
East0 Port
REQ
East1 Port
REQ
West0 Port
REQ
West1 Port
REQ
South0 Port
REQ
South1 Port
REQ
IPE
REQ
OPE
North CP Arbiter
1104
REQ
North Port

Fig. 11

Select Register For Control Port(CP) North0

Reset State: 0000 0000 0000 0000

RID Bit #	Name	Description/Purpose	Read/Write
15–10	Reserved	Reserved And Should Be Written As Zeros	Write
9–7	CP_R_SEL(n)	CP Receiver Select Bits	Read/Write
6–3	Reserved	Reserved And Should Be Written As Zeros	Write
2–0	CP_R_SEL(n)	CP Receiver Select Bits	Read/Write

Value	Selection	Description/Purpose
000	OPE	Command From OPE is Transmitted
001	East0	Command From East0 Port Is Transmitted
010	East1	Command From East1 Port Is Transmitted
011	South0	Command From South0 Port Is Transmitted
100	South1	Command From South1 Port Is Transmitted
101	West0	Command From West0 Port Is Transmitted
110	West1	Command From West1 Port Is Transmitted
111	IPE	Command From IPE Is Transmitted

Value	Selection	Description/Purpose
001	East0	East0 Port Receives Command
010	East1	East1 Port Receives Command
011	South0	South0 Port Receives Command
100	South1	South1 Port Receives Command
101	West0	West0 Port Receives Command
110	West1	West1 Port Receives Command

Fig. 12